

**GOVT. COLLEGE OF ENGINEERING & TECHNOLOGY, BIKANER**  
**DEPARTMENT OF COMPUTER SCIENCE & ENGINEERING**  
**TIME TABLE (SESSION 2016-17)**  
**B.TECH. III Semester CSE-1**

<b>Time</b>	<b>8:00-8:50</b>	<b>8:50-9:40</b>	<b>9:40-10:30</b>	<b>10:30-11:20</b>	<b>11:20-12:10</b>	<b>12:10-1:00</b>
<b>Day</b>						
<b>Monday</b>	EDC Lab :-B1 Batch (EC Deptt.)			OOPS (ASP)	EDC (EC Deptt.)	Math (Maths Deptt.)
	DE Lab : -B2 Batch (EC Deptt.)	Library(B2)				
<b>Tuesday</b>	EDC Lab :-B2 Batch (EC Deptt.)			Math (Maths Deptt.)	OOPS (ASP)	EDC (EC Deptt.)
	DE Lab : -B3 Batch (EC Deptt.)	Library(B3)				
<b>Wednesday</b>	EDC Lab :-B3 Batch (EC Deptt.)			EDC (EC Deptt.)	Math (Maths Deptt.)	OOPS (ASP)
	DE Lab : -B1 Batch (EC Deptt.)	Library(B1)				
<b>Thursday</b>	DSA Lab:- B1 Batch (KP)			DSA (KP)	Linux (DY)	DE (EC Deptt.)
	Unix Shell Prog.:-B2 Batch(DY)	Math(T)B2				
	C++ Lab :-B3 Batch (ASP)					
<b>Friday</b>	DSA Lab:- B2 Batch (KP)			DE (EC Deptt.)	DSA (KP)	Linux (DY)
	Unix Shell Prog.:-B3 Batch(DY)	Math(T)B3				
	C++ Lab :-B1 Batch (ASP)					
<b>Saturday</b>	DSA Lab:- B3 Batch (KP)			Linux (DY)	DE (EC Deptt.)	DSA (KP)
	Unix Shell Prog.:-B1 Batch(DY)	Math(T)B1				
	C++ Lab :-B2 Batch (ASP)					

**ASP:** Dr. Ajeet Singh Poonia, **DY:** Dharmendra Yadav, **KP:** Kapil Pandey.

CC:PA to Principal  
 Academic Coordinator  
 Head: CSE, ECE & Mathematics

Time Table I/C

**GOVT. COLLEGE OF ENGINEERING & TECHNOLOGY, BIKANER**  
**DEPARTMENT OF COMPUTER SCIENCE & ENGINEERING**  
**TIME TABLE (SESSION 2016-17)**  
**B.TECH. III Semester CSE-2**

Time	8:00-8:50	8:50-9:40	9:40-10:30	10:30-11:20	11:20-12:10	12:10-1:00
Day						
<b>Monday</b>	DSA Lab:- A1 Batch (SC)			Linux (KS)	DSA (SC)	DE (EC Deptt.)
	Unix Shell Prog.:-A2 Batch(KS)		Math(T)A2			
<b>Tuesday</b>	DSA Lab:- A2 Batch (SC)			DE (EC Deptt.)	Linux (KS)	DSA (SC)
	Unix Shell Prog.:-A3 Batch(KS)		Math(T)A3			
<b>Wednesday</b>	DSA Lab:- A3 Batch (SC)			DSA (SC)	DE (EC Deptt.)	Linux (KS)
	Unix Shell Prog.:-A1 Batch(KS)		Math(T)A1			
<b>Thursday</b>	C++ Lab :-A1 Batch (LS)			OOPS (LS)	EDC (EC Deptt.)	Math (Maths Deptt.)
	EDC Lab :-A2 Batch (EC Deptt.)					
	DE Lab :-A3 Batch (EC Deptt.)		Library(A3)			
<b>Friday</b>	C++ Lab :-A2 Batch (LS)			Math (Maths Deptt.)	OOPS (LS)	EDC (EC Deptt.)
	EDC Lab :-A3 Batch (EC Deptt.)					
	DE Lab :-A1 Batch (EC Deptt.)		Library(A1)			
<b>Saturday</b>	C++ Lab :-A3 Batch (LS)			EDC (EC Deptt.)	Math (Maths Deptt.)	OOPS (LS)
	EDC Lab :-A1 Batch (EC Deptt.)					
	DE Lab :-A2 Batch (EC Deptt.)		Library(A2)			

KS: Kartar Singh, LS:Laxman Singh, SC: Sunita Choudhary.

CC:  
PA to Principal  
Academic Coordinator  
Head, CSE,ECE & Mathematics

(Time Table I/C)

**GOVT. COLLEGE OF ENGINEERING & TECHNOLOGY, BIKANER**  
**DEPARTMENT OF COMPUTER SCIENCE & ENGINEERING**  
**TIME TABLE (SESSION 2016-17)**  
**B.TECH. VII Semester CSE-1**

<b>TIME</b>	<b>8:00-8:50</b>	<b>8:50-9:40</b>	<b>9:40-10:30</b>	<b>10:30-11:20</b>	<b>11:20-12:10</b>	<b>12:10-1:00</b>
<b>Day</b>						
<b>Monday</b>	ADBMS (Elective Y)	Cloud Computing (AP)	ISS (DY)	Compiler Design Lab :-B1 Batch (X)		
				Web Design Lab :-B2 Batch (DY)		
<b>Tuesday</b>	ISS (DY)	ADBMS (Elective Y)	Cloud Computing (AP)	Compiler Design Lab :-B2 Batch(X)		
				Web Design Lab :-B3 Batch (DY)		
<b>Wednesday</b>	Cloud Computing (AP)	ISS (DY)	ADBMS (Elective Y)	Compiler Design Lab :-B3 Batch (X)		
				Web Design Lab :-B1 Batch ( )		
<b>Thursday</b>	CC (X)	DMWH	CAD for VLSI (EC Deptt.)	VLSI Physical Design Lab:-B1 Batch(EC Deptt.)		
				Minor Project Lab(B2)		PD
				Practical Training Seminar:- B3 Batch		
<b>Friday</b>	CAD for VLSI (EC Deptt.)	CC (X)	DMWH	VLSI Physical Design Lab:-B2 Batch(EC Deptt.)		
				Minor Project Lab(B3)		PD
				Practical Training Seminar :- B1 Batch		
<b>Saturday</b>	DMWH	CAD for VLSI (EC Deptt.)	CC (X)	VLSI Physical Design Lab:-B3 Batch(EC Deptt.)		
				Minor Project Lab(B1)		PD
				Practical Training Seminar:- B2 Batch		

AP:Abhishek Purohit, DY: Dharmendra Yadav,X,Y:Guest Faculty.

(Time-Table I/C)

CC:  
PA to Principal  
Academic Coordinator  
Head, ECE

**GOVT. COLLEGE OF ENGINEERING & TECHNOLOGY, BIKANER**  
**DEPARTMENT OF COMPUTER SCIENCE & ENGINEERING**  
**TIME TABLE (SESSION 2016-17)**  
**B.TECH. VII Semester CSE-2**

<b>TIME</b>	<b>8:00-8:50</b>	<b>8:50-9:40</b>	<b>9:40-10:30</b>	<b>10:30-11:20</b>	<b>11:20-12:10</b>	<b>12:10-1:00</b>
<b>DAY</b>						
<b>Monday</b>	ADBMS (Elective X)	ISS (GK)	CAD for VLSI (EC Deptt.)	VLSI Physical Design Lab:-A1 Batch (EC Deptt.)		
				Web DesignLab :-A2 Batch (AP)		
<b>Tuesday</b>	CAD for VLSI (EC Deptt.)	ADBMS (Elective X)	ISS (GK)	VLSI Physical Design Lab:-A2 Batch (EC Deptt.)		
				Web DesignLab :-A3 Batch (AP)		
<b>Wednesday</b>	ISS (GK)	CAD for VLSI (EC Deptt.)	ADBMS (Elective X)	VLSI Physical Design Lab:-A3 Batch (EC Deptt.)		
				Web DesignLab :-A1 Batch (AP)		
<b>Thursday</b>	CC (y)	DMWH (KS)	Cloud Computing (NC)	Compiler Design Lab :-A1 Batch (y)		
				Minor Project Lab(A2)		PD
				Practical Training Seminar:- A3 Batch		
<b>Friday</b>	Cloud Computing (NC)	CC (y)	DMWH (KS)	Compiler Design Lab :-A1 Batch (y)		
				Minor Project Lab(A3)		PD
				Practical Training Seminar:- A1 Batch		
<b>Saturday</b>	DMWH (KS)	Cloud Computing (NC)	CC (y)	Compiler Design Lab :-A1 Batch (y)		
				Minor Project Lab(A1)		PD
				Practical Training Seminar:- A2 Batch		

**AP:**Abhishek Purohit,**GK:** Gagandeep Kaur, **KS:** Kartar Singh,**NC:** Neeraj Choudhary. **X,Y:**Guest Faculty.

(Time-Table I/C)

CC:  
PA to Principal  
Academic Coordinator  
Head: CSE & ECE

**GOVT. COLLEGE OF ENGINEERING & TECHNOLOGY, BIKANER**  
**DEPARTMENT OF COMPUTER SCIENCE & ENGINEERING**  
**TIME TABLE (SESSION 2016-17)**  
**B.TECH. V Semester CSE-1**

DAY	TIME	8:00-8:50	8:50-9:40	9:40-10:30	10:30-11:20	11:20-12:10	12:10-1:00
<b>Monday</b>		DLD (EC Deptt.)	CA (LS)	ITC (EC Deptt.)	System Design in UML Lab.:A1 Batch(JB)		
					Operating Systems Simulation Lab: A2 Batch(GK)		
<b>Tuesday</b>		ITC (EC Deptt.)	DLD (EC Deptt.)	CA (LS)	System Design in UML Lab.:A2 Batch(JB)		
					Operating Systems Simulation Lab: A3 Batch(GK)		
<b>Wednesday</b>		CA (LS)	ITC (EC Deptt.)	DLD (EC Deptt.)	System Design in UML Lab.:A3 Batch(JB)		
					Operating Systems Simulation Lab: A1 Batch(GK)		
<b>Thursday</b>		TF (EC Deptt.)	OS (SC)	DBMS (DD)	DBMS Lab: A1 Batch(DD)		
					Digital Hardware Design Lab: A2 Batch(EC Deptt.)		
<b>Friday</b>		OS (SC)	DBMS (DD)	TF (EC Deptt.)	DBMS Lab: A2 Batch(DD)		
					Digital Hardware Design Lab: A3 Batch(EC Deptt.)		
<b>Saturday</b>		DBMS (DD)	TF (EC Deptt.)	OS (SC)	DBMS Lab: A3 Batch(DD)		
					Digital Hardware Design Lab: A1 Batch(EC Deptt.)		

**DD: Devender Daila,JB: Jai Bhaskar, LS:Laxman Singh ,SC: Sunita Choudhary,GK:Gagandeep Kaur**

(Time-Table I/C)

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**B.TECH. V Semester CSE-2**

TIME	8:00-8:50	8:50-9:40	9:40-10:30	10:30-11:20	11:20-12:10	12:10-1:00
DAY						
<b>Monday</b>	TF (EC Deptt.)	DBMS (NC)	ITC (EC Deptt.)	DBMS Lab: B1 Batch(NC)		
				Digital Hardware Design Lab: B2 Batch(EC Deptt.)		
<b>Tuesday</b>	ITC (EC Deptt.)	TF (EC Deptt.)	DBMS (NC)	DBMS Lab: B2 Batch(NC)		
				Digital Hardware Design Lab: B3 Batch(EC Deptt.)		
<b>Wednesday</b>	DBMS (NC)	ITC (EC Deptt.)	TF (EC Deptt.)	DBMS Lab: B3 Batch(NC)		
				Digital Hardware Design Lab: B1 Batch(EC Deptt.)		
<b>Thursday</b>	DLD (EC Deptt.)	OS (JB)	CA (GK)	Operating Systems Simulation Lab: B1 Batch(JB)		
				System Design in UML Lab.:B2 Batch(AP)		
<b>Friday</b>	OS (JB)	CA (GK)	DLD (EC Deptt.)	Operating Systems Simulation Lab: B2 Batch(JB)		
				System Design in UML Lab.:B3 Batch(AP)		
<b>Saturday</b>	CA (GK)	DLD (EC Deptt.)	OS (JB)	Operating Systems Simulation Lab: B3 Batch(GK)		
				System Design in UML Lab.:B1 Batch(AP)		

**AP:**Abhishek Purohit,**GK:** Gagandeep Kaur, **JB:** Jai Bhaskar, **NC:** Neeraj Choudhary.

(Time-Table I/C)

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