5CS1 COMPUTER ARCHITECTURE Class: V Sem.

B.Tech. Evaluation Branch: Computer Engg.

Schedule per Week Lectures: 3

Examination Time = Three (3) Hours Maximum Marks = 100 [Mid-term (20) & End-term (80)]

Units Contents of the subject

Unit I

Introduction to Computer Architecture and Organization. Von Neuman Architecture, Flynn Classification,Register Transfer and Micro operations: Register transfer language, memory transfers.Arithmetic,Micro-operations, Logic Micro-operations, Shift Micro-operations, Bus and memory transfers.Computer Organization and Design: Instruction cycle, computer registers,common bus system, computer instructions, addressing modes, design of a basic computer.

Unit II

Central Processing Unit: General register organization, stack organization,Instruction Pipeline and Vector processing: Pipeline structure, speedup, efficiency,formats, Data transfer and manipulation, program control.RISC, CISC characteristics.throughput and bottlenecks. Arithmetic pipeline and Instruction pipeline.

Unit III

Computer Arithmetic: Adder, Ripple carry Adder, carry look Ahead Adder,Multiplication: Add and Shift, Array multiplier and Booth Multiplier, Division:restoring and Non-restoring Techniques. Floating Point Arithmetic: Floating point representation, Add, Subtract, Multiplication, Division.

Unit IV

Memory Organization: RAM, ROM, Memory Hierarchy, Organization,Associative memory, Cache memory, and Virtual memory: Paging and Segmentation.

Unit V

Input-Output Organization: Input-Output Interface, Modes of Transfer, Priority Interrupt, DMA, IOP processor.

Syllabus Covered (In Bold fonts)

Unit I

Introduction to Computer Architecture and Organization. Von Neuman Architecture, Flynn Classification,Register Transfer and Micro operations: Register transfer language, memory transfers.Arithmetic,Micro-operations, Logic Micro-operations, Shift Micro-operations, Bus and memory transfers.Computer Organization and Design: Instruction cycle, computer registers,common bus system, computer instructions, addressing modes, design of a basic computer.

Unit II

Central Processing Unit: General register organization, stack organization,Instruction Pipeline and Vector processing: Pipeline structure, speedup, efficiency,formats, Data transfer and manipulation, program control.RISC, CISC characteristics.throughput and bottlenecks. Arithmetic pipeline and Instruction pipeline.

Unit III

Computer Arithmetic: Adder, Ripple carry Adder, carry look Ahead Adder,Multiplication: Add and Shift, Array multiplier and Booth Multiplier, Division:restoring and Non-restoring Techniques. Floating Point Arithmetic: Floating point representation, Add, Subtract, Multiplication, Division.

Unit IV

Memory Organization: RAM, ROM, Memory Hierarchy, Organization,Associative memory, Cache memory, and Virtual memory: Paging and Segmentation.

Unit V

Input-Output Organization: Input-Output Interface, Modes of Transfer, Priority Interrupt, DMA, IOP processor.